We Claim:

1. A system for transparently programming a clock and date recovery circuit in an optical–electrical-optical (OEO) switch comprising:
   a means to receive and convert an optical signal to an electrical signal;
   a CDR (clock and data recovery) circuit to resynchronize the electrical signal;
   a monitoring circuit to analyze the quality of the data eye pattern of the resynchronized signal; and
   a processor to calculate a predicted bit error rate (BER) based on the data eye pattern and to provide feedback to the CDR circuit.

2. The system as defined in claim 1 wherein the received signal has a range of frequencies.

3. The system as defined in claim 2 wherein the processor programs the CDR to select and phase locks onto a first frequency.

4. The system as defined in claim 3 wherein the processor determines whether the first frequency is correct based on the quality of the data eye pattern.

5. The system as defined in claim 4 wherein if the first frequency is not the correct frequency the processor programs the CDR circuit to a new frequency and to monitor the data eye pattern of the new frequency.

6. The system as defined in claim 5 wherein said the processor programs the CDR circuit to scan through the frequencies until the correct frequency is selected.

7. The system as defined in claim 6 wherein the processor programs the CDR circuit to first select and lock onto the lowest frequency of the received data signal.

8. A method of transparently programming a clock and date recovery circuit in an (OEO) optical –electrical-optical switch comprising:
receiving an optical data signal at a system input and converting said optical signal to an electrical data signal;
resynchronizing the electrical data signal with a CDR (clock and data recovery) circuit;
monitoring the data eye pattern of the resynchronized data signal to determine its quality;
predicting, in a processor, a bit error rate (BER) based on the data eye pattern; and
providing feedback to the CDR circuit.

9. The method as defined in claim 8 wherein the received optical data signal has a range of frequencies.

10. The method as defined in claim 9 wherein the processor programs the CDR to select a first frequency.

11. The method as defined in claim 10 wherein the processor checks to determine whether the CDR is phase locked onto the first frequency and if so checks the predicted BER of the resynchronized signal.

12. The method as defined in claim 10 wherein the processor checks to determine whether the CDR is phase locked onto the first frequency and if not programs the CDR to select a new frequency.

13. The method as defined in claim 11 wherein if the predicted BER of the resynchronized signal is correct the CDR is programmed to accept the first frequency.

14. The method as defined in claim 12 wherein the processor programs the CDR to lock onto the new frequency and the step of checking the predicted BER is repeated.

15. The method as defined in claim 14 wherein the processor programs further frequencies into the CDR and the steps repeated until the correct BER is detected.